Dr. ASHISH MAURYA

Assistant Professor, ECE Department

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Ph.D Department of Electronics Engineering, IIT-ISM Dhabad — **April 2023**

EDUCATION

M.Tech in VLSI Design, IIIT, Gwalior (M.P) — **June 2017**

B.Tech in Electronics and Communication Engineering — **June 2014**

Feroze Gandhi Inst. of Engg. and Tech., Raebareli (U.P)

TECHNICAL SKILLS

Languages: Python, Verilog, VerilogA, C, C++, Embedded Assembly.

Simulation Tools: Sentaurus TCAD, Cadence Virtuoso, Xilinx ISE, Xilinx Vivado, Synopsys Tools (Design Compiler, Tetramax, IC Compiler, HSPICE and Prime-Time), SILVACO Tools (SmartSPICE, Gateway, Atlas & Expert), ATK-VNL, Mentor Graphics ModelSim and MATLAB.

ACHIEVEMENTS & SCHOLARSHIP

- **UGC-NET** qualified for Assistant Professor (2017)
- **GATE Scholarship from Ministry of Human Resource and Development, GOI.**
  GATE-2015, Percentile Obtained: 97.41

POSITIONS OF RESPONSIBILITY

- **Assistant Dean Academincs (R&D)**, KIT Kanpur
- **Senior Project Associate**, Department of Electrical Engineering, IIT Kanpur
- **Project Leader**, Project of FPGA Implementation of real time speech codec under SMDP - C2SD project at IIIT Gwalior, GOI.
- **Teaching Assistant**, VLSI Design Lab, ABV-IIITM Gwalior under the supervision of Prof. G. K. Sharma and Prof. Manisha Pattanaik.
- Volunteer in **IEEE International Symposium on Nanoelectronic and Information Systems (IEEE-iNIS) - 2016** held in ABV-IIITM, Gwalior.

PUBLICATIONS (ORCiD: 0000-0002-6374-1813)

Transactions/Journals:

1. **Ashish Maurya**, et al., "Investigation of Source Region's Random Doping Fluctuation Effects on Analog and RF Performance in All-Si DG-TFET," in ***IEEE Transactions on Electron Devices***, 2022. DOI: 10.1109/TED.2022.3193992.
2. **Ashish Maurya**, et al., "Investigation of Single-Event-Transient Effects Induced by Heavy-ion in all-Silicon DG-TFET," in ***IEEE Access***, 2022, DOI: 10.1109/ACCESS.2022.3213685.
3. **Ashish Maurya**, et al., "Surface Orientated <100>, <110>, and <111> Silicon-based Double-Gate Tunnel-FET for Linearity and Analog/RF Performance Analysis," in ***Silicon***, 2022. DOI: 10.1007/s12633-022-02232-2.
4. **Ashish Maurya**, et al., "Implementation and Performance Analysis of Low Power 1 GHz 4-bit Flash ADC using III-V Tunnel-FET," in ***Circuits, Systems, and Signal Processing (CSSP)***, 2022. DOI: 10.1007/s00034-022-02187-0.
5. **Ashish Maurya**, et al., "Half Intake Track-by-Track Search Algorithm for CS-ACELP based G.729 Speech Codec," in ***Journal of Engineering Science & Management Education***", vol. 10, no. 1, pp. 8-13, 2017. DOI: 10.13140/RG.2.2.11884.21128.
6. Pankaj Kumar, **Ashish Maurya**, et al., "Assessment of Negative Bias Temperature Instability due to Interface and Oxide Trapped Charges in Gate-all-around TFET," *in* ***IEEE Transactions on Nanotechnology*** *(2023). DOI: 10.1109/TNANO.2023.3255012.*
7. Pankaj Kumar, **Ashish Maurya**, et al., "Analog and RF performance optimization for gate all around tunnel FET using broken-gap material," *in* ***Scientific Reports*** *(2022),* DOI: 10.1038/s41598-022-22485-6.
8. Pankaj Kumar, **Ashish Maurya**, et al., "Assessment of interface trapped charge induced threshold voltage hysteresis effect in gate-all-around TFET," *in* ***Micro and Nanostructures*** *(2022),* DOI: 10.1016/j.micrna.2022.207502.

Conferences:

1. **Ashish Maurya**, et al., "Performance Analysis of Compound III-V Semiconductor Materials based MOSFET," *2022 IEEE 9th Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON)*, 2022, pp. 1-6, doi: 10.1109/UPCON56432.2022.9986476.
2. **Ashish Maurya**, et al., "Calculation of OFF-Current of Tunnel FETs based on Sub-threshold Swing: A New Approach," *2020 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*, Bangalore, India, 2020, pp. 1-4. DOI: 10.1109/CONECCT50063.2020.9198675.
3. Pankaj Kumar, Kalyan Koley, Rupam Goswami, **Ashish Maurya** and Subindu Kumar, "Assessment of hot carrier stress induced threshold voltage shift in gate-all-around MOSFETs," *2022 IEEE 19th India Council International Conference (INDICON), Kochi, India, 2022, pp. 1-4, doi: 10.1109/INDICON56171.2022.10039693.*
4. Pankaj Kumar, Kalyan Koley, Rupam Goswami, **Ashish Maurya** and Subindu Kumar, "Electrical Noise Behaviour of High-k Gate-All-Around MOSFET Based on Two-Port Device Network Analysis," *2022 14th International Conference on Information Technology and Electrical Engineering (ICITEE)*, 2022, pp. 68-72, doi: 10.1109/ICITEE56407.2022.9954118.
5. Bhawana Kumari, **Ashish Maurya**, Manisha Pattanaik and G. K. Sharma, "An efficient algebraic codebook structure for CS-ACELP based speech codecs," *2017 8th IEEE International Conference on Computing, Communication and Networking Technologies (ICCCNT)*, Delhi, 2017, pp. 1-6. DOI: 10.1109/ICCCNT.2017.8203957.